CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of fabricating a strained semiconductor-on-insulator (SSOI) comprising the steps of:

forming a second crystalline semiconductor layer that is strained on a surface of a first crystalline semiconductor layer, said first crystalline semiconductor layer is located atop an insulating layer of a preformed silicon-on-insulator (SOI) substrate;

subjecting the preformed SOI substrate containing the second crystalline semiconductor layer to a first annealing step at a first temperature that is sufficient to relax the strain in the second crystalline semiconductor layer;

performing an amorphization ion implantation to create a buried amorphized region comprising the entirety of the first crystalline semiconductor layer and a lower portion of the second crystalline semiconductor layer;

subjecting the preformed SOI substrate containing the second crystalline semiconductor layer and the buried amorphized region to a second annealing step at a second temperature sufficient to recrystallize the buried amorphized region resulting in said first crystalline semiconductor layer recrystallizing in a strained state; and

selectively removing the second crystalline semiconductor layer providing a strained semiconductor-on-insulator substrate.

2. The method of Claim 1 wherein the insulating layer is a crystalline or non-crystalline oxide or nitride that is highly resistant to Ge diffusion.

3. The method of Claim 1 wherein the first crystalline semiconductor layer has thickness from about 5 to about 50 nm.

4. The method of Claim 1 wherein the first crystalline semiconductor layer comprises Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, another III/V or II/VI compound semiconductor.

5. The method of Claim 4 wherein the first crystalline semiconductor layer is a Si-containing semiconductor.

6. The method of Claim 1 wherein the second crystalline semiconductor layer comprises Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, another III/V or II/VI compound semiconductor.

7. The method of Claim 6 wherein the second crystalline semiconductor layer is a Ge-containing material.

8. The method of Claim 7 wherein the Ge-containing material is a SiGe alloy or pure Ge.

9. The method of Claim 1 wherein forming the second crystalline semiconductor layer comprises an epitaxial growth process.

10. The method of Claim 9 wherein the epitaxial growth process is selected from rapid thermal chemical vapor deposition, low-pressure chemical vapor deposition, ultra-high vacuum chemical vapor deposition, atmospheric pressure chemical vapor deposition, molecular beam epitaxy and plasma-enhanced chemical vapor deposition.

11. The method of Claim 1 wherein the second crystalline semiconductor layer has a thickness from about 10 to about 500 nm.

12. The method of Claim 1 further comprising performing a defect creating ion implantation to create defects within or near the first crystalline semiconductor layer between said forming and first annealing step.

13. The method of Claim 12 wherein the defect creating ion implantation is carried out using ions of hydrogen, deuterium, helium, oxygen, neon, boron, silicon or mixtures and isotopes thereof.

14. The method of Claim 13 wherein the ions are hydrogen or oxygen ions.

15. The method of Claim 12 wherein the defect creating ion implantation is carried out using an ion concentration of below 3E16 cm^{-2}.

16. The method of Claim 12 wherein the defects can serve as efficient discloation nucleation sites which allow the second crystalline semiconductor layer to relax more efficiently.

17. The method of Claim 12 wherein the defect creating ion implantation is performed using an implantation mask.

18. The method of Claim 1 wherein the first annealing step is performed in an inert gas ambient or a forming gas ambient.

19. The method of Claim 1 wherein the first temperature of the first annealing step is from about 700°C to about 1100°C.

20. The method of Claim 1 wherein the first annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process of a spike anneal.

21. The method of Claim 1 wherein the amorphization ion implantation is carried out using ions selected from Si, P, As, Ge, C and any combination thereof.

22. The method of Claim 1 wherein the second annealing step is performed in an inert gas ambient or a forming gas ambient.

23. The method of Claim 1 wherein the second temperature of the second annealing step is from about 600°C to about 1100°C.

24. The method of Claim 1 wherein the second annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process of a spike anneal.

25. The method of Claim 1 wherein the selectively removing comprises chemical etching, reactive ion etching, low-temperature oxidation, atomic oxidation, chemical mechanical polishing, gas-cluster beam thinning or any combination thereof.

26. A method of fabricating a strained semiconductor-on-insulator (SSOI) comprising the steps of:

forming a second crystalline semiconductor layer that is strained on a surface of a first crystalline semiconductor layer, said first crystalline semiconductor layer is located atop an insulating layer of a preformed silicon-on-insulator (SOI) substrate;

performing a defect creating ion implantation to create defects within or near the first crystalline semiconductor layer;

subjecting the preformed SOI substrate containing the second crystalline semiconductor layer and the defects to a first annealing step at a first temperature that is sufficient to relax the strain in the second crystalline semiconductor layer;

performing an amorphization ion implantation to create a buried amorphized region comprising the entirety of the first crystalline semiconductor layer and a lower portion of the second crystalline semiconductor layer;

subjecting the preformed SOI substrate containing the second crystalline semiconductor layer and the buried amorphized region to a second annealing step at a second temperature sufficient to recrystallize the buried amorphized region resulting in said first crystalline semiconductor layer recrystallizing in a strained state; and

selectively removing the second crystalline semiconductor layer providing a strained semiconductor-on-insulator substrate.

27. The method of Claim 26 wherein the insulating layer is a crystalline or non-crystalline oxide or nitride that is highly resistant to Ge diffusion.

28. The method of Claim 26 wherein the first crystalline semiconductor layer has thickness from about 5 to about 50 nm.

29. The method of Claim 26 wherein the first crystalline semiconductor layer comprises Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, another III/V or II/VI compound semiconductor.

30. The method of Claim 29 wherein the first crystalline semiconductor layer is a Si-containing semiconductor.

31. The method of Claim 26 wherein the second crystalline semiconductor layer comprises Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, another III/V or II/VI compound semiconductor.

32. The method of Claim 31 wherein the second crystalline semiconductor layer is a Ge-containing material.

33. The method of Claim 32 wherein the Ge-containing material is a SiGe alloy or pure Ge.

34. The method of Claim 26 wherein forming the second crystalline semiconductor layer comprises an epitaxial growth process.

35. The method of Claim 34 wherein the epitaxial growth process is selected from rapid thermal chemical vapor deposition, low-pressure chemical vapor deposition, ultra-high vacuum chemical vapor deposition, atmospheric pressure chemical vapor deposition, molecular beam epitaxy and plasma-enhanced chemical vapor deposition.

36. The method of Claim 26 wherein the second crystalline semiconductor layer has a thickness from about 10 to about 500 nm.

37. The method of Claim 26 wherein the defect creating ion implantation is carried out using ions of hydrogen, deuterium, helium, oxygen, neon, boron, silicon or mixtures and isotopes thereof.

38. The method of Claim 37 wherein the ions are hydrogen or oxygen ions.

39. The method of Claim 26 wherein the defect creating ion implantation is carried out using an ion concentration of below 3E16 cm^{-2}.

40. The method of Claim 26 wherein the defects can serve as efficient dislocation nucleation sites which allow the second crystalline semiconductor layer to relax more efficiently.

41. The method of Claim 26 wherein the defect creating ion implantation is performed using an implantation mask.

42. The method of Claim 26 wherein the first annealing step is performed in an inert gas ambient or a forming gas ambient.

43. The method of Claim 26 wherein the first temperature of the first annealing step is from about 700°C to about 1100°C.

44. The method of Claim 26 wherein the first annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process or a spike anneal.

45. The method of Claim 26 wherein the amorphization ion implantation is carried out using ions selected from Si, P, As, Ge, C and any combination thereof.

46. The method of Claim 26 wherein the second annealing step is performed in an inert gas ambient or a forming gas ambient.

47. The method of Claim 26 wherein the second temperature of the second annealing step is from about 600°C to about 1100°C.

48. The method of Claim 26 wherein the second annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process or a spike anneal.

49. The method of Claim 26 wherein the selectively removing comprises chemical etching, reactive ion etching, low-temperature oxidation, atomic oxidation, chemical mechanical polishing, gas-cluster beam thinning or any combination thereof.

50. A method of fabricating a strained Si-on-insulator (SSOI) comprising the steps of:

forming a Ge-containing layer that is strained on a surface of a Si-containing layer, said Si-containing layer is located atop an insulating layer of a preformed silicon-on-insulator (SOI) substrate;

subjecting the preformed SOI substrate containing the Ge-containing to a first annealing step at a first temperature that is sufficient to relax the strain in the Ge-containing layer;

performing an amorphization ion implantation to create a buried amorphized region comprising the entirety of the Si-containing layer and a lower portion of the Ge-containing layer;

subjecting the preformed SOI substrate containing the Ge-containing layer and the buried amorphized region to a second annealing step at a second temperature sufficient to recrystallize the buried amorphized region resulting in said Si-containing layer recrystallizing in a strained state; and

selectively removing the Ge-containing layer providing a strained Si-containing-on-insulator substrate.

51. The method of Claim 50 wherein the insulating layer is a crystalline or non-crystalline oxide or nitride that is highly resistant to Ge diffusion.

52. The method of Claim 50 wherein the Si-containing layer has thickness from about 5 to about 50 nm.

53. The method of Claim 50 wherein the Ge-containing layer is a SiGe alloy or pure Ge.

54. The method of Claim 50 wherein the forming the Ge-containing layer comprises an epitaxial growth process selected from rapid thermal chemical vapor deposition, low-pressure chemical vapor deposition, ultra-high vacuum chemical vapor deposition, atmospheric pressure chemical vapor deposition, molecular beam epitaxy and plasma-enhanced chemical vapor deposition.

55. The method of Claim 50 wherein the Ge-containing layer has a thickness from about 10 to about 500 nm.

56. The method of Claim 50 further comprising performing a defect creating ion implantation to create defects within or near the first crystalline semiconductor layer between said forming and first annealing step.

57. The method of Claim 56 wherein the defect creating ion implantation is carried out using ions of hydrogen, deuterium, helium, oxygen, neon, boron, silicon or mixtures and isotopes thereof.

58. The method of Claim 57 wherein the ions are hydrogen or oxygen ions.

59. The method of Claim 57 wherein the defect creating ion implantation is carried out using an ion concentration of below 3E16 cm^{-2}.

60. The method of Claim 57 wherein the defects can serve as efficient dislocation nucleation sites which allow the second crystalline semiconductor layer to relax more efficiently.

61. The method of Claim 57 wherein the defect creating ion implantation is performed using an implantation mask.

62. The method of Claim 50 wherein the first annealing step is performed in an inert gas ambient or a forming gas ambient.

63. The method of Claim 50 wherein the first temperature of the first annealing step is from about 700°C to about 1100°C.

64. The method of Claim 50 wherein the first annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process or a spike anneal.

65. The method of Claim 50 wherein the amorphization ion implantation is carried out using ions selected from Si, P, As, Ge, C and any combination thereof.

66. The method of Claim 50 wherein the second annealing step is performed in an inert gas ambient or a forming gas ambient.

67. The method of Claim 50 wherein the second temperature of the second annealing step is from about 600°C to about 1100°C.

68. The method of Claim 50 wherein the second annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process or a spike anneal.

69. The method of Claim 50 wherein the selectively removing comprises chemical etching, reactive ion etching, low-temperature oxidation, atomic oxidation, chemical mechanical polishing, gas-cluster beam thinning or any combination thereof.